

are steadily replacing their mechanical and hydraulic predecessors. As the sophistication of these systems grows, their complexity has grown dramatically as well, creating difficulties in the application of traditional engineering m ...

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4	A VHDL compiler based on attribute grammar methodology					
0	R. Farrow, A. G. Stanculescu June 1989 ACM SIGPLAN Notices, Proceedings of the ACM SIGPLAN 1989 Conference					
	on Programming language design and implementation PLDI '89, Volume 24					
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	This paper presents aspects of a compiler for a new hardware description language (VHDL) written using attribute grammar techniques. VHDL is introduced, along with the new compiler challenges brought by a language that extends an Ada subset for the purpose of describing hardware. Attribute grammar programming solutions are presented for some of the language challenges. The organization of the compiler and of the target virtual machine represented by the simulation kernel are disc					
5	Hardware/software co-design: VHDL and Ada 95 code migration and integrated analysis					
November 1998 ACM SIGAda Ada Letters, Proceedings of the 1998 annual ACM SIGAda international conference on Ada SIGAda '98, Volume XVIII						
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6	COMP: a VHDL composition system	Г				
٩	P. R. Jordan, R. D. Williams					
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	An automated system for creating and managing VHDL design units is described in this paper. This system helps the hardware designer to learn the syntax of the VHSIC Hardware Description Language (VHDL) and to produce code which can be used for simulations. This demonstration prototype tool is written in C to run on a Sun workstation, and it produces IEEE standard 1076 VHDL code.					
7	The IBM VHDL design system	Γ				
③	L. F. Saunders October 1987 Proceedings of the 24th ACM/IEEE conference on Design automation	_				
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	This paper presents the IBM VHDL Design System. This set of Computer Aided Engineering (CAE) design tools, built around the VHSIC Hardware Description Language (VHDL) and developed for IBM internal use, along with other design automation tools, is used by IBM design engineers to develop computer hardware. The function and operation of each piece					

⁸ An interface between VHDL and EDIF

discussed.

of the system is described. IBM usage and some of the problems encountered are also

\$	M. Shahdad October 1987 Proceedings of the 24th ACM/IEEE conference on Design automation	
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	The VHSIC Hardware Description Language (VHDL) and the Electronic Design Interchange Format (EDIF) are becoming industry standards for hardware design and documentation. Potential users of these standards are interested in understanding the application range of each standard and the way each standard relates to the other. This paper presents scenarios in which VHDL and EDIF can contribute to different aspects of the design process, as well as the technical issues in providing a design inter	
9	VHDL teamwork, organization units and workspace management	
	S. Olcoz, L. Ayuda, I. Izaguirre, O. Penalba February 1998 Proceedings of the conference on Design, automation and test in Europe	
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	A new set of tools for Teamwork, Organization Units, Workspace and Build management of VHDL-based reusable components, organized in libraries, accessible through an heterogeneous and distributed environment is presented. These tools support the collaborative and distributed development of systems-on-a-chip reusing VHDL components available through the intranets and the Internet. They must be used as a complementary support to the design tools (simulation, synthesis, etc.) already available in th	
	Keywords : Teamwork, cooperative work, workspace, management, VHDL analysis, elaboration, simulation.	
10	A VHDL error simulator for functional test generation	
③	Alessandro Fin, Franco Fummi January 2000 Proceedings of the conference on Design, automation and test in	
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11	Translation of VHDL to Ada Carl F. Schaefer March 1987 Proceedings of the Joint Ada conference fifth national conference on Ada technology and fourth Washington Ada Symposium	
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12	An overview of VHDL language and technology	
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	resulting in a hardware descrindustry. Version 7.2 of the laconsidered by the IEEE as a proposed standard based on	gy has been under development for the past five years, iption language that enjoys widespread support within the anguage was released in August of 1985 and is being prime candidate for standardization. It is expected that a Version 7.2 will be available in January of 1987. This standard DL Tutorial containing extensive example	
13 ②		VHDL-AMS using denotational semantics I, J. P. Bowen, R. France, M. Lorrondo Petrie, C. Delgado	
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15		synthesis of verified hardware descriptions in VHDL	
②	Sánchez Fernández	elgado, Andrés López Marín, Natividad Martínez Madrid, Luis n Programming Languages and Systems (TOPLAS),	
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